CLAIMS:

What is claimed is:

1. An integrated circuit comprising:

a memory array having a first side;

a self-timing signal-producing circuit located at the first side;

a self-timing signal-reading circuit located at the first side; and

a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array.

2. The integrated circuit of claim 1, wherein the self-timing signal-producing circuit is a dummy row decoder circuit.

3. The integrated circuit of claim 1, wherein the self-timing signal-producing circuit is a dummy memory cell.

4. The integrated circuit of claim 3, wherein the self-timing signal-reading circuit is a dummy sense amplifier.

5. The integrated circuit of claim 1, wherein the memory array is a segment of a larger segmented memory array.

6. The integrated circuit of claim 5, wherein the larger segmented memory array includes a second segment, and the second segment made up of memory cells that are disabled through metal programming.

7. The integrated circuit of claim 6, further comprising:

a second routing path, wherein the second routing path is routed over the second segment.

8. The integrated circuit of claim 1, further comprising:

a programmable logic circuit coupled to the memory array, wherein the memory array outputs data as a single column of bit lines and the programmable logic circuit is programmed to derive a word of a desired word size from the single column of bit lines.

9. The integrated circuit of claim 8, wherein the programmable logic circuit is programmed to behave as a multiplexer and the word of the desired word size is derived from the single column of bit lines by the multiplexer's selecting a subset of the bit lines from the single column of bit lines.

10. The integrated circuit of claim 1, wherein the routing path extends into the memory array to a point that is at some intermediate location between the first side and a second side of the memory array, such that a wire delay associated with the routing path approximates a wire delay that would be experienced on a hypothetical routing path extending from the first side to the second side.

11. A method comprising:

receiving design characteristics for an integrated circuit application requiring a memory space;

providing an integrated circuit layout of a memory array having a first side;

selecting a portion of the memory array to be used as the memory space for the integrated circuit application;

incorporating into the integrated circuit layout a self-timing signal-producing circuit located at the first side;

incorporating into the integrated circuit layout a self-timing signal-reading circuit located at the first side;

incorporating into the integrated circuit layout a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array.

12. The method of claim 11, further comprising:

eliminating a metal routing layer from an unused portion of the memory array.

13. The method of claim 12, further comprising:

incorporating a metal routing path into the integrated circuit layout, such that metal routing path is routed over the unused portion of the memory array, but is not connected to unused memory cells in the unused portion of the memory array.

14. The method of claim 11, further comprising:

receiving a desired word size for the memory space;

generating a logic circuit design coupled to the portion of the memory array such that the logic circuit design allows the portion of the memory array to be accessed using the desired word size.

15. The method of claim 14, wherein the logic circuit design is generated as a program for a programmable logic circuit.

16. A computer program product in a computer-readable medium comprising functional descriptive material that, when executed by a computer, causes the computer to perform actions that include:

receiving design characteristics for an integrated circuit application requiring a memory space;

providing an integrated circuit layout of a memory array having a first side;

selecting a portion of the memory array to be used as the memory space for the integrated circuit application;

incorporating into the integrated circuit layout a self-timing signal-producing circuit located at the first side;

incorporating into the integrated circuit layout a self-timing signal-reading circuit located at the first side;

incorporating into the integrated circuit layout a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array.

17. The computer program product of claim 16, comprising additional functional descriptive material that, when executed by a computer, causes the computer to perform additional actions that include:

eliminating a metal routing layer from an unused portion of the memory array.

18. The method of claim 17, comprising additional functional descriptive material that, when executed by a computer, causes the computer to perform additional actions that include:

incorporating a metal routing path into the integrated circuit layout, such that metal routing path is routed over the unused portion of the memory array, but is not connected to unused memory cells in the unused portion of the memory array.

19. The method of claim 16, comprising additional functional descriptive material that, when executed by a computer, causes the computer to perform additional actions that include:

receiving a desired word size for the memory space;

generating a logic circuit design coupled to the portion of the memory array such that the logic circuit design allows the portion of the memory array to be accessed using the desired word size.

20. The computer program product of claim 19, wherein the logic circuit design is generated as a program for a programmable logic circuit.